| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 8 | "error check and correction" | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:07 |
| 2 | 9 | ("error check and correction" or ECC) same (ECC adj2 memory adj2 cell adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 3 | 488 | ("error check and correction" or ECC) and (ECC adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 4 | 9 | ("error check and correction" or ECC) and (ECC adj2 memory adj2 cell adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 5 | 9 | (ECC adj2 memory adj2 cell adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 6 | 2 | ("error check and correction" or ECC) and (ECC adj2 memory) and wordlines and bitlines | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:10 |
| 7 | 16 | ("error check and correction" or ECC) and wordlines and bitlines | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:15 |
| 8 | 286 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:17 |
| 9 | 265 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 10 | 8 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 11 | 6 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 12 | 6 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:19 |
| 13 | 0 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 14 | 0 | ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 15 | 4 | ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 17 | 10 | (ECC adj2 memory) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:21 |
| 16 | 5 | (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:35 |
| 18 | 0 | (ECC adj2 memory adj2 cell$1) and (wordline$1 adj2 decoder) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:28 |
| 19 | 5 | (ECC adj2 memory adj2 cell$1) and ("X" adj2 decoder) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:29 |

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| 20 | 890 | ECC and (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:36 |
| 22 | 3300 | ("X" or "Y") adj decoder$1 | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:37 |
| 23 | 47839 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") or ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 24 | 53706 | decoder$1 and ((word adj1 line$1) or "WL") or ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 25 | 9729 | decoder$1 and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 26 | 1166 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 27 | 24 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") and (ECC and (semiconductor adj2 memory) ) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 28 | 29 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") and ECC | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:49 |
| 29 | 38 | ECC near4 memory near4 cell$1 near4 array | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:50 |
| 30 | 8 | ECC adj2 cell$1 adj2 array | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:50 |
| 21 | 237 | ECC same (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:54 |
| 31 | 63 | (ECC near5 design$4) and (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:59 |
| 32 | 18 | ECC and (design near10 (semiconductor adj2 memory)) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:00 |
| 33 | 556 | ECC and (error adj2 recovery) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:01 |
| 34 | 14 | ECC and (error adj2 recovery) and (semiconductor adj2 device) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:04 |
| 35 | 493 | (arrang$5 or dispos$5) near20 ECC | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:04 |
| 36 | 4 | (arrang$5 or dispos$5) near20 (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:09 |
| 37 | 11 | (arrang$5 or dispos$5) same (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:09 |

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| 4 | 9 | ("error check and correction" or ECC) and (ECC adj2 memory adj2 cell adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 5 | 9 | (ECC adj2 memory adj2 cell adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:09 |
| 6 | 2 | ("error check and correction" or ECC) and (ECC adj2 memory) and wordlines and bitlines | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:10 |
| 7 | 16 | ("error check and correction" or ECC) and wordlines and bitlines | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:15 |
| 8 | 286 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:17 |
| 9 | 265 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 10 | 8 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 11 | 6 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:18 |
| 12 | 6 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:19 |
| 13 | 0 | ("error check and correction" or ECC) and ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 14 | 0 | ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory adj2 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 15 | 4 | ((word adj1 lines) or "WL") and ((bit adj1 lines) or "BL") and decod$3 and (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:20 |
| 17 | 10 | (ECC adj2 memory) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:21 |
| 16 | 5 | (ECC adj2 memory adj2 cell$1 adj2 array) and (semiconductor adj2 memory) and (normal adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:35 |
| 18 | 0 | (ECC adj2 memory adj2 cell$1) and (wordline$1 adj2 decoder) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:28 |
| 19 | 5 | (ECC adj2 memory adj2 cell$1) and ("X" adj2 decoder) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:29 |

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| 24 | 53706 | decoder$1 and ((word adj1 line$1) or "WL") or ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 25 | 9729 | decoder$1 and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 26 | 1166 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 27 | 24 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") and (ECC and (semiconductor adj2 memory) ) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:40 |
| 28 | 29 | (("X" or "Y") adj decoder$1) and ((word adj1 line$1) or "WL") and ((bit adj1 lines) or "BL") and ECC | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:49 |
| 29 | 38 | ECC near4 memory near4 cell$1 near4 array | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:50 |
| 30 | 8 | ECC adj2 cell$1 adj2 array | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:50 |
| 21 | 237 | ECC same (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:54 |
| 31 | 63 | (ECC near5 design$4) and (semiconductor adj2 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 11:59 |
| 32 | 18 | ECC and (design near10 (semiconductor adj2 memory)) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:00 |
| 33 | 556 | ECC and (error adj2 recovery) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:01 |
| 34 | 14 | ECC and (error adj2 recovery) and (semiconductor adj2 device) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:04 |
| 35 | 493 | (arrang$5 or dispos$5) near20 ECC | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:04 |
| 36 | 4 | (arrang$5 or dispos$5) near20 (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:09 |
| 37 | 11 | (arrang$5 or dispos$5) same (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:16 |
| 38 | 156 | (arrang$5 or dispos$5) same (ECC adj4 circuit) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:22 |
| 39 | 56 | (arrang$5 or dispos$5) near10 (ECC adj4 circuit) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:17 |
| 40 | 11 | (arrang$5 or dispos$5) same (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:23 |
| 41 | 4 | (arrang$5 or dispos$5) near10 (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:26 |
| 42 | 3496673 | portion$1 (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:27 |

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| 44 | 5 | portion$1 same (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:27 |
| 43 | 4 | portion$1 near20 (ECC adj4 cell$1) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:42 |
| 45 | 48 | (ECC adj1 mode) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:48 |
| 46 | 796 | (ECC adj3 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:48 |
| 47 | 221 | (ECC adj1 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:49 |
| 48 | 4 | (arrang$5 or design$5 or set$4 or implemen$4 or fabricat$5) adj5 (ECC adj1 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:53 |
| 49 | 24 | (arrang$5 or design$5 or set$4 or implemen$4 or fabricat$5) near10 (ECC adj1 memory) | USPAT; EPO; JPO; DERWENT | 2003/12/07 12:53 |